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Design of CMOS Devices Using TANNER EDA

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Abstract:
Today's computers, CPUs and cell phone make use of CMOS technology due to several key advantages. CMOS offer low power dissipation, relatively high speed, high noise margin. So, here we are designing CMOS inverter and performing transient analysis using TANNER EDA Software. For that firstly we are designing schematic diagram in S-edit and to observe its truth table we move onto corresponding T-spice after that the desired waveform is observed in W-edit. The layout is designed in L-edit.

Key words: *CMOS, inverter, low power dissipation, high speed, TANNER EDA, S-edit, T-spice, W-edit, L-edit*

1. Introduction

VLSI is an implementation technology for electronic circuitry, either analog or digital. There are many application of VLSI in day to day life, such as microprocessor, memory etc. This technology has made highly sophisticated control system mass-producable and therefore cheap. In digital logic, the inverter is truly the nucleus of all digital designs. Once its operation and properties are clearly understood, designing more intricate structures such as logic gates, adders, multiplexers and microprocessor is greatly simplified [5]. CMOS technology first proposed in the 1960's. CMOS is referred to as complementary-symmetry metal–oxide–semiconductor. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.
Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is drawn when the transistors in the CMOS device are switching between on and off states. CMOS inverter consists of PMOS and NMOS working as complementary switches.

2. Types of Analysis

2.1. DC Analysis

- The DC analysis is helpful in determining the required power supply and its limits, the current consumption and to be sure that all the devices in the circuit are working in the safe region without exceeding their normal rating.
- From the dc analysis, we can determine the node voltage, mesh current and branch voltage and branch current of a network.

2.2. AC Analysis

- Ac analysis is helpful in determining the resonance condition, Phase angle, Q-factor, dissipation factor, maximum and minimum impedance, etc.
- AC analysis is small signal analysis and It is used in microelectronic.

2.3. Transient Analysis

- In the time domain you need to make transient analysis to measure the rise/fall times, slew rate, etc.
- Transient analysis is helpful in determining the charging and discharging time of capacitor and inductor, transient behavior of series & parallel circuit & steady state error.

3. Inverter

An inverter is a logic gate which complements the given input.

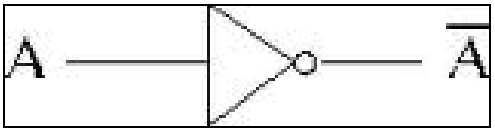

Figure 1: Symbol of Inverter.

INPUT	OUTPUT
0 (0V)	1 (5V)
1 (5V)	0 (0V)

Table 1: Truth Table

Inverter circuit serves as the basic logic gate to swap between the two voltage levels (0v and +5v). The Inverter can be made using discrete transistors. The NOT gate is often called as Inverter. It can be fabricated at low cost.

4. CMOS Inverter

CMOS (complementary-symmetry metal–oxide–semiconductor) inverter contains PMOS and NMOS transistor. CMOS inverters are one of the most widely used and adaptable MOSFET inverter. It is used for chip designing.

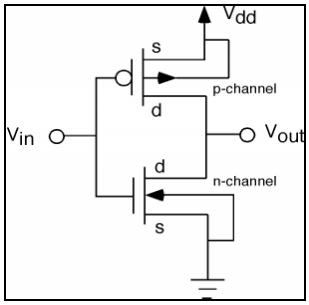

Figure 2: CMOS Inverter.

A supply voltage VDD is connected at source terminal of PMOS and GND is connected to source terminal of NMOS. The gate and drain terminals of PMOS and NMOS transistor are connected together.

4.1. Working of CMOS inverter

- For small values of the input voltage,(Vin=0v), the NMOS transistor is switched off, whereas the PMOS transistor is switched on and connects the output mode to VDD (VDD=5v).

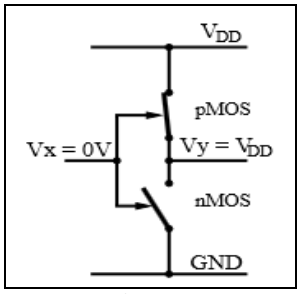

Figure 3

- For large values of the input voltage,(Vin=5v), the PMOS transistor is switched off, whereas the NMOS transistor is switched on and connects the output mode to GND (GND= 0v).

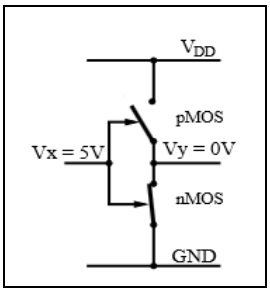

Figure 4

- The high and low output level equal VDD and GND, respectively; in other word, the voltage swing is equal to the supply voltage. This results in high noise margin [5].
- In steady state, there always a path is present with finite resistance in between the output and either VDD or GND. A well-designed CMOS inverter will have low output impedance, which makes it less sensitive to noise and other disturbances.

4.2. Characteristics

The working of the CMOS inverter can be studied through transfer and current characteristics as shown in Figure 5.

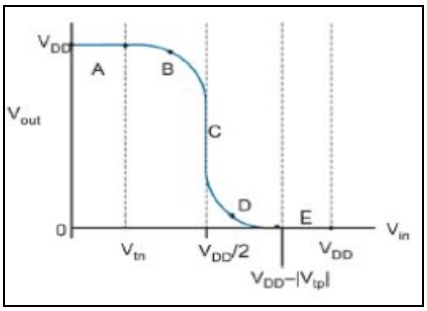

Figure 5

- In region A, where Vin lies between 0 and Vtn i.e. threshold voltage of NMOS transistor the NMOS is cutoff and operation of PMOS is linear and resulting output voltage is equal to VDD.
- In region B, the input voltage is increased beyond Vtn. The NMOS transistor starts conducting in saturation mode and output voltage begins to decrease.
- In region C, the input voltage is equal to VDD/2. Both NMOS and PMOS transistors enter into saturation mode and output voltage drops sharply.
- In region D, Vin lies between VDD/2 and VDD - |Vtp |. The NMOS transistor starts to operate in linear mode.
- In region E, the input voltage is greater than VDD - |Vtp|. The PMOS transistor is cutoff and output voltage is equal to 0.

5. Software Tool

TANNER EDA helps to transform your ideas into design. It has created a software platform that is cost efficient. It is powerful enough to handle complex design. TANNER EDA's continued innovation makes its tools effective solution that grows with a company as its performance needs change. TANNER EDA consist of various tools namely S-edit, T-spice, W-edit, L-edit and LVS.

5.1. S-edit

In S-Edit, schematic design of circuit enables you to check your design for common errors such as undriven nets, unconnected pins and nets driven by multiple outputs so you can catch errors early before running simulations.

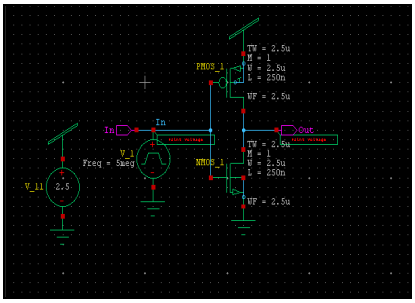

Figure 6

5.2. T-spice

T-Spice lets you precisely characterize circuit behavior using virtual data measurements. For greater efficiency and productivity, T-Spice controls over your simulation process with an easy-to-use graphical interface.

5.3. W-edit

The W-Edit waveform analysis tool is a comprehensive viewer for comparing, displaying and analyzing simulation results. W-Edit is dynamically linked to T-Spice and S-Edit with a run-time update feature that displays simulation results as they are being generated and allows waveform cross-probing directly in the schematic editor for faster design cycles.

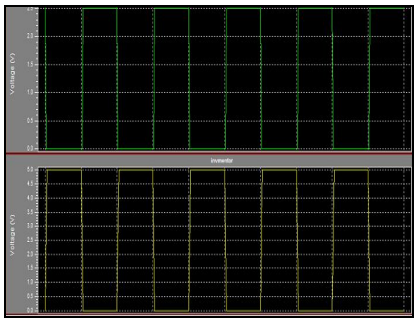

Figure 7

5.4. L-edit

Layout is essentially a drawing process. L-Edit gives you the flexibility and control you need to master the editing process.

5.5. LVS

LVS (Layout versus Schematic) compares netlist generated by schematic and netlist generated by layout. The generated parameters are compared and if found similar then it is an indication that the designed layout is ready for fabrication.

6. Simulation Results

6.1. Inverter

- Schematic in TANNER 6

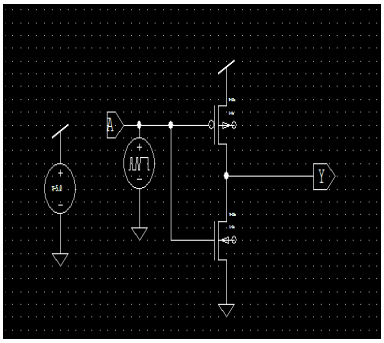

Figure 8

- WAVEFORM

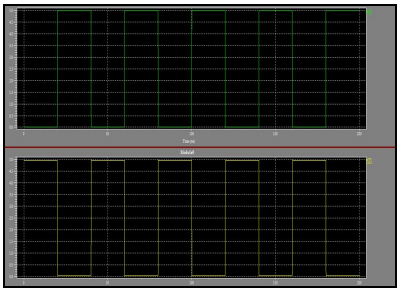

Figure 9

6.2. NAND Gate

In digital electronics, a NAND Gate is a logic gate which produce an output that is false if an only if all its input are true and is also known as Negated AND or NOT AND.

- Schematic in TANNER 6

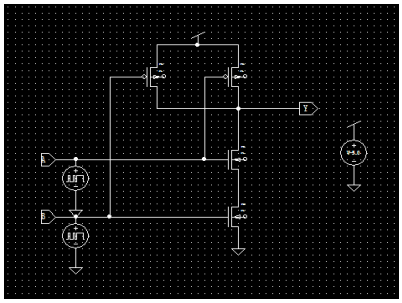

Figure 10

- WAVEFORM

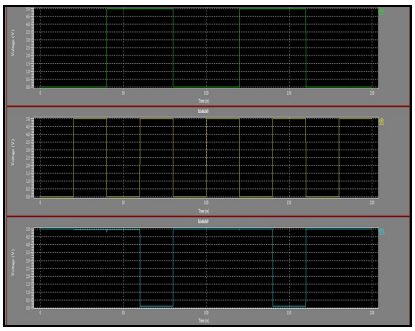

Figure 11

6.3. NOR Gate

The NOR gate have a high output only when both the inputs are low and have low output when one or more input are high.

- Schematic in TANNER 6

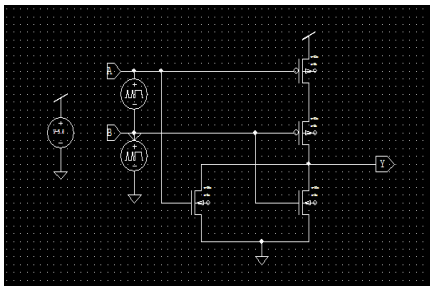

Figure 12

- WAVEFORM

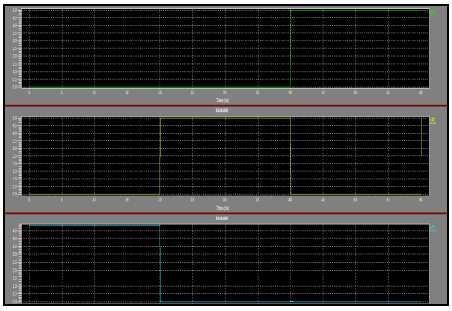

Figure 13

6.4. Power Measurement

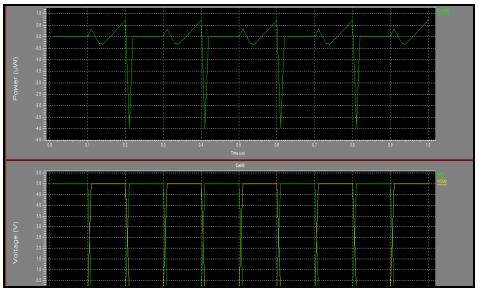

Figure 14

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