THE INTERNATIONAL JOURNAL OF SCIENCE & TECHNOLEDGE

Diffusion of Phosphorus in Silicon Thin Films by Spin and Dip Coating

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Abstract:

In this work, Spin coating and Dip coating techniques are used for the diffusion of phosphorus in silicon in order to realize the emitter of a silicon solar cell which is a very important and critical step in photovoltaic technology. Several techniques are used for the realization of n+p junctions among which the ionic implantation, vapor phase diffusion and diffusion from solid sources are the most common. In this work, the emitter is made by diffusion of solid doping sources that we elaborated by the sol gel method associated with spin coating and dip coating on silicon wafers. The doping solutions were prepared by the sol gel method using tetraethoxysilane "TEOS" and methyltriethoxysilane "MTEOS" and phosphoric acid H_3PO_4 as a precursor by emulsion of phosphoric acid in isopropanol. This experience allowed us to study the electrical properties of the emitters using the four-point technique. The measurement results showed that the values of the sheet resistance $R_{\square}$ obtained by dip coating are comparable to those obtained with the spin coating technique.

Keywords: Phosphorus diffusion, solid doping sources, Spin coating, dip coating, sol gel

1. Introduction

The diffusion process of the n+p emitter is a critical and expensive step in the manufacture of silicon solar cells. Gaseous diffusion from a $POCl_3$ source is a technique widely used in the photovoltaic and microelectronics industry [1, 2, 3, 4, 5]. In this technique, the control of technological parameters, such as gas pressure and flow in an open tube furnace is crucial for the quality of the transmitter and the improvement of the cell's conversion efficiency. While the cost of photovoltaic solar cells is identified as the main barrier preventing their wide use, alternative technologies have often been studied to look for simple methods characterized by a continuous production rate, allowing one to optimize the cost / efficiency ratio and make this source of clean energy more attractive. The screen-printing technique, generally used for the metallization of the front and rear contacts, has been extended to phosphorus doping to obtain the n+p electrical junction and also to deposit the antireflection layers [6]. Deposition techniques such as Chemical Spraying, also called Spray [7, 8, 9, 10, 11], Spin Coating [12, 13, 14, 15] and Dip Coating [16, 17, 18, 19] are also widely used now to realize of the n+p emitter on silicon substrates. This last technique is simple to carry out and can be promising. Its features (simplicity, low cost) can be of paramount importance to ensure the sustainable development of a photovoltaic industry in developing countries where sophisticated and expensive equipment is rarely available. In our previous work [20], the Spin coating technique was used for the realization of the n+p and n+pp+ electrical junctions by diffusion of the solid sources that we developed by the sol gel method. In this contribution, this work is continued by using Spin coating and Dip coating techniques.

2. Materials and Methods

The solutions were prepared by the sol gel method. The reagents used for the n⁺ junction is methyltriethoxysilane "MTEOS" or tetraethoxysilane (TEOS), phosphoric acid H₃PO₄ and isopropanol. The total volume set for this study is 20 ml with 5.2 ml of TEOS or MTEOS 12.6 ml of isopropanol and 2.2 ml of a solution of phosphoric acid. 5.2 ml of TEOS or MTEOS are then added to the half of required amount of isopropanol. A second mixture is prepared from 6.3 ml of isopropanol and 2.2 ml of phosphoric acid; then the two solutions obtained are mixed. The resulting mixture is refluxed with stirring at 82°C for two hours.

The substrates used for the deposits are polycrystalline and monocrystalline silicon substrates cleaned with 10% hydrofluoric acid (HF).

The deposit is made by using the Spin coating technique [20] and the technique of coating by immersion of the substrate (Dip Coating). The dip coating process has been used since 1939 to produce thin films in sol-gel technology [21]. It has also been used to produce thin films in other technologies, such as photosensitive resin films [22] and lubricant layers for magnetic hard disks [23]. The Dip Coating is a simple process for depositing a thin film of the solution on a plate, a cylinder, or an irregularly shaped object. The fact that the geometry of the substrates can vary widely is a distinctive feature of this technique. In addition, it makes it possible to adjust the microstructure (porosity, crystallinity) of the deposits and to control their thickness [24]. In this sol gel technique, the substrate is simply immersed in the solution containing the "soil" and withdrawn under very controlled and stable conditions to obtain a film of regular thickness. During the ascent, the liquid will flow on the substrate and at the end of the flow, the substrate is covered with a uniform and porous film. The process can be repeated several times to obtain a thicker layer. Some factors such as the viscosity of the solution, the rate of substrate shrinkage, the temperature and drying time, and the number of repetitions influence the results.

The stabilization of the layer after the deposit is made by drying at 150°C for 30 min for the spin coating and at 200°C for 60 min for the dip coating to evaporate the solvent and the diffusion is carried out in a conventional furnace at different temperatures (850, 900, 950 and 1000°C) and at different annealing times (15, 30, 45 and 60 min).

Figure 1 summarizes the flowchart of the development and characterization used in this work.

Figure 1: Experimental Procedure Used for the Junction Realization and Electrical Characterization

3. Results and Discussion

The electrical characterizations of the n⁺p emitters are carried out by the four-point method, in Table 1 below, the results of the square resistances for different temperatures are represented.

Techniques	Annealing temperature into ° C / 45min	Sheet resistance into Ω/□	
		Side A	Side B
Dip Coating (sol gel)	850	144,99	132,84
	900	46,27	53,86
	950	23,57	23,78
	1000	7,86	8,13
Spin Coating (sol gel)	850	175,60	
	900	50,37	
	950	26,14	
	1000	9,82	

Table 1: Results of Square Resistance Measurements for Different Temperatures

The results presented in Table 1 indicate that the value of the sheet resistance depends on the deposit technique adopted. However, whatever the technique, the values obtained show that there is a diffusion of phosphorus from the solid diffusion sources deposited into the silicon surface. The sheet resistance values are between 9.82 and 175.60 Ω to temperatures ranging from 850 to 1000 $^{\circ}\text{C}$ for the spin coating. Similar results are obtained with the dip coating. Here, the values of the square resistance are between 7.86 and 158.72 Ω / sq for the side A and between 8.88 and 149.19 Ω / sq for the side B, which also shows the use of this deposit technique for achieving the solid doping sources form of thin films on the silicon surface. Furthermore, dip coating is a simple process for depositing a thin film of solution onto a plate, cylinder, or irregular-shaped object but here the temperature and the drying time are higher than that of the spin coating. In the figures below are represented the square resistances as a function of the temperature for the dip coating (Figure 2) and spin coating (Figure 3).

Figure 2 : Sheet Resistance as a Function of Temperature
(N+P Junction Realized by the Dip Coating Technique)

Figure 3 : Sheet Resistance as a Function of Temperature
(N+P Junction Realized by the Spin Coating Technique)

They show a decrease in the sheet resistance when the annealing temperature increases. This decrease can be explained by the fact that when the annealing temperature is not high enough, the phosphorus impurity can be considered as immobile, so the phosphorus atoms will not have enough force to penetrate inside silicon and recombine on the surface of the silicon substrate which leads to a high sheet resistance. But if the annealing temperature is sufficiently high, under the effect of thermal agitation, the atoms are movable and can move inside the silicon substrate which leads to a decrease in sheet resistance.

We have also studied the effect of the thermal annealing time on the square resistors, in Table 2 below, the results of the sheet resistances for different annealing times are presented by setting the annealing temperature at 900 $^{\circ}\text{C}$.

Substrates	Annealing Times in min with T=900°C	Sheet Resistance into $\Omega/\square$	
		Side A	Side B
Dip Coating (sol gel)	30	105,15	103,43
	45	58,06	60,76
	60	46,17	50,10
	75	45,71	39,44
Spin Coating (sol gel)	15	167,79	
	20	137,11	
	25	105,50	
	30	56,07	

Table 2: Results of Sheet Resistance Measurements for Different Annealing Times

The values obtained after the characterizations also show that there is diffusion of phosphorus from the solid diffusion sources deposited on the surface of the silicon. It can also be observed that the diffusion time for the junctions produced by the dip coating technique is higher than those produced by the spin coating technique

In the figures below are represented the square resistances as a function of the Annealing time for the spin coating technique (Figure 4) and the dip coating technique (Figure 5).

Figure 4: Sheet Resistance as a Function of Annealing Time (N+P Junction Realized by Spin Coating)

Figure 5: Sheet Resistance as a Function of Annealing Time (N+P Junction Realized By Dip Coating)

Figures 4 and 5 also show a decrease in sheet resistance as the annealing time increases. We can also note here that for the high diffusion times, the charge carriers have enough energy to penetrate further inside the silicon substrate which then causes a reduction of the square resistance.

4. Conclusion

We were able to make the n+p electrical junction from the solid sources of phosphorus diffusion in silicon using the sol-gel method. The results obtained by measuring the sheet resistance show a good diffusion of the phosphorus atoms

inside the silicon substrate. In addition, we were able to show that the spin coating and dip coating techniques can be used for the realization of the electrical junction. It has been observed that the temperature, the drying time and the diffusion time for the junctions produced by the dip coating technique are higher than those produced by the spin coating technique

5. Acknowledgements

The authors are grateful to the reviewers for the constructive reviews. This research did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors.

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